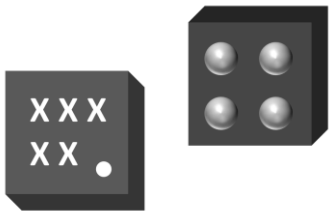
3-Axis Single Chip Magnetic Sensor

The QMC6309H is a three-axis magnetic sensor, which integrates magnetic sensors and signal condition ASIC into one silicon chip. This wafer level chip scale package (WLCSP) is targeted for applications such as e-compass, map rotation, gaming and personal navigation in mobile and wearable devices.



The QMC6309H is based on state-of-the-art, high resolution, magneto-resistive technology. Along with the custom-designed 16-bit ADC ASIC, it offers the advantages of low noise, high accuracy, low power consumption, offset cancellation and temperature compensations. QMC6309H enables 1° to 2° compass heading accuracy. The I²C serial bus allows for easy interface.

The QMC6309H is in a 0.8x0.8x0.5mm3 surface mount 4-pin WLCSP package.

FEATURES

- 3-Axis Magneto-Resistive Sensors in a 0.8x0.8x0.5 mm^3 WLCSP, Guaranteed to Operate Over an Extended Temperature Range of -40 °C to +85 °C.
- 16 Bit ADC With Low Noise AMR Sensors Achieves 2 milli-Gauss Field Resolution
- Wide Magnetic Field Range (±32 Gauss)
- I^3C bus Interface with I^2C embedded, compliant with MIPI I^3C v1.0 specification
- In-band interrupts (IBI)
- Temperature Compensated Data Output
- Built-In Self-Test
- Built-In FIFO
- Wide Range Operation Voltage (1.62V to 3.6V) and low Power Consumption less 10uA at 1Hz ODR
- Lead Free Package Construction
- Software and Algorithm Support Available

BENEFIT

- Small Size for Highly Integrated Products. Signals Have Been Digitized and Calibrated.
- Enables 1° To 2° Degree Compass Heading Accuracy, Allows for Pedestrian Navigation and LBS Applications
- Maximizes Sensor's Full Dynamic Range and Resolution
- Automatically Maintains Sensor's Sensitivity Under Wide Operating Temperature Range
- Enables Low-Cost Functionality Test After Assembly in Production
- Compatible with Battery Powered Applications
- RoHS Compliance
- Compassing Heading, Hard Iron, Soft Iron, and Auto Calibration Libraries Available

CONTENTS

1. INTERNAL SCHEMATIC DIAGRAM

1.1 Internal Schematic Diagram

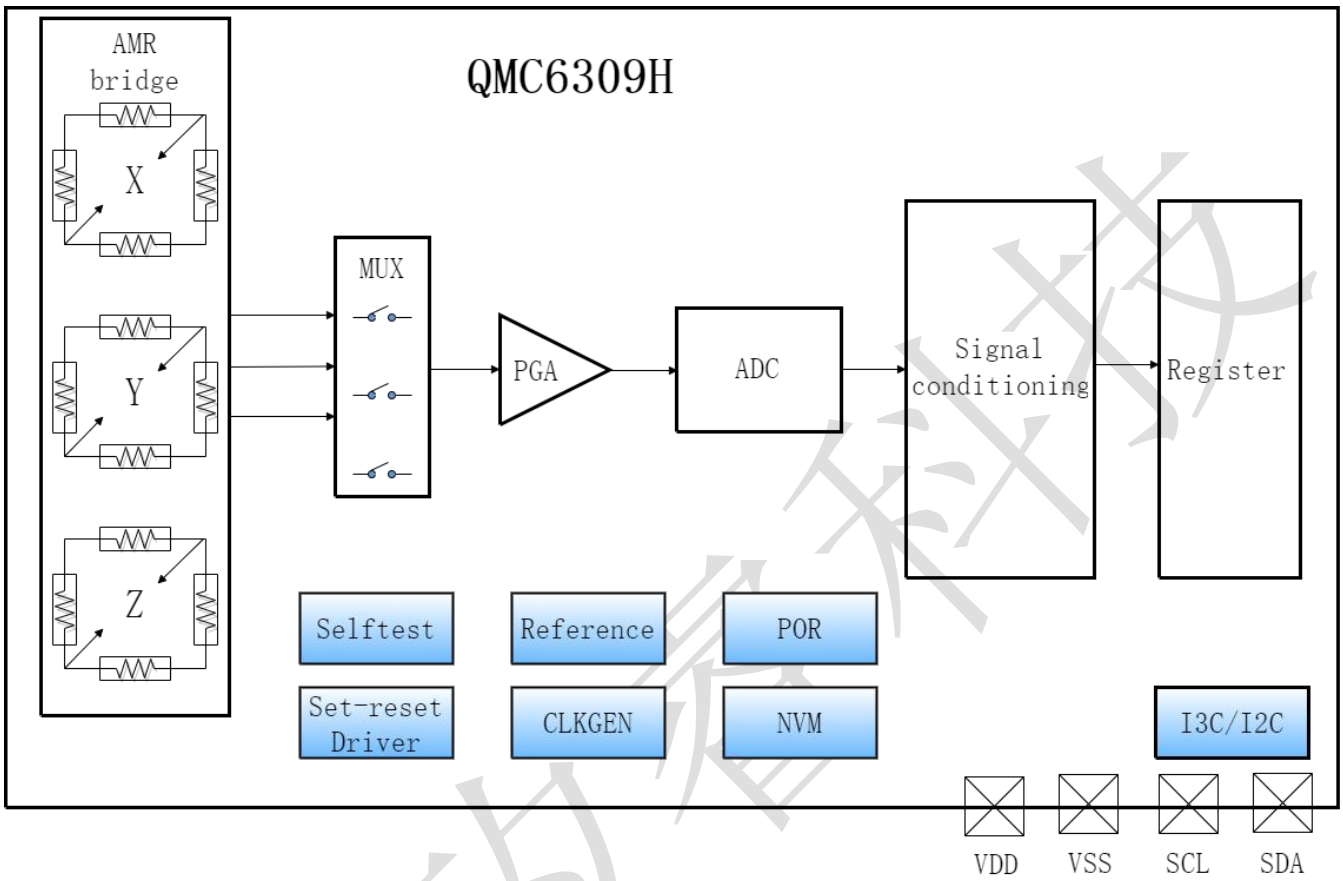


Figure 1. Block Diagram

1.2 Block Functions

Table 1. Block Functions

Block	Function
AMR bridge	3-axis magnetic sensor
MUX	Multiplexer for sensor channels
PGA	Programmable gain amplifier for sensor signals
ADC	Analog-to-Digital converter
Signal conditioning	Digital blocks for magnetic signal calibration and compensations
I^3C/I^2C	Interface logic data I/O
NVM	Non-volatile memory
Register	Internal register
Set-reset Driver	Internal driver to initialize magnetic sensor
Reference	Voltage/current reference for internal biasing
CLKGEN.	Internal oscillator for internal operation
POR	Power on reset

2. SPECIFICATIONS AND I/O CHARACTERISTICS

2.1 Product Specifications

Table 2. Specifications (Tested and specified at 25°C, VDD=1.8V, except stated otherwise.)

Parameter	Conditions		Min	Typ	Max	Unit
Supply Voltage	VDD		1.62	1.8	3.6	V
I^2C Input Voltage[5]	VDDIO		1.08	1.8	VDD	V
I^3C Input Voltage[6]				1.8	VDD	V
Suspend Mode Current	Total Current on VDD			1.0		μA
Normal Mode Current [1]	Low power and high power mode	ODR=1Hz		3/10		uA
		ODR=10Hz		30/100		
		ODR=50Hz		150/500		
		ODR=100Hz		300/1000		
		ODR=200Hz		600/2000		
Continuous Mode Current[3]	OSR1=1	Maximum ODR		3200		uA
Sensor Field Range	Full Scale		-32		32	Gauss
Sensitivity[2],[3]	±32G		-5		5	%
	Field Range = ±32G			1000		LSB/G
	Field Range = ±16G			2000		LSB/G
	Field Range = ±8G			4000		LSB/G
Linearity[3]	Field Range = ±32G Happlied= ±16G			0.6		%FS
Hysteresis[3]	3 sweeps across ±32G			0.03		%FS
Offset[4]			-1		1	Gauss
Sensitivity Tempco[3]	Ta = -40°C~85°C				±0.05	%/°C
Digital Resolution	Field Range = ±32G			1.0		mGauss
Field Resolution[3]	OSR=8,8			2.5		mGauss
	OSR=8,4			3.5		mGauss
	OSR=8,2			5.0		mGauss
	OSR=8,1			7.0		mGauss
X-Y-Z Orthogonality[3]	Sensitivity Directions			90±1	90±3	Degree
Operating Temperature			-40		85	°C
ESD	HBM		2000			V
	CDM		500			

Notes:
1. The Normal Mode Current differs at different OSR1 setting. The value of low power mode is measured at setting OSR1=1 and the value of high power mode is measured at OSR1=8.
2. Sensitivity is calibrated at zero field; it is slightly decreased at high fields.
3. Based on 3lots characterization results at continuous mode
4. Null Field Output
5. VDDIO support 1.08V when VDD=1.8V or equal to VDD
6. I^3C test at continuous mode

2.2 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings (VSS=0)

Parameter	MIN.	MAX.	Unit
VDD	-0.5	5	V
Storage Temperature	-40	125	°C
Exposed to Magnetic Field (all directions)		10000	Gauss
Reflow Classification	MSL 1, 260 °C Peak Temperature		

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

2.3 I/O Characteristics

Table 4. I/O Characteristics (VDD =VDDIO= 1.8V, Tested at 25°C)

Parameter(Units)	Symbol	Min.	Typ.	Max.	Unit
High Level Input Voltage	V_{IH}	0.7*VDDIO			V
Low Level Input Voltage	V_{IL}	0		0.3*VDDIO	V
Hysteresis of Schmitt Trigger Input [1]	V_{HYS}	0.1*VDDIO			V
Input Leakage, All Inputs	I_{IL}	-10		10	uA
High Level output Voltage [2]	V_{OH}	0.8*VDDIO			V
Low Level output Voltage [3]	V_{OL}			0.2*VDDIO	V

Notes:
1. Schmitt trigger input (reference value for design).
2. Output is Push-Pull.
3. Output is Open-Drain and Push-Pull. Connect a pull-up resistor externally in Open-Drain mode.

3. PACKAGE PIN CONFIGURATIONS

3.1 Package 3-D View

Arrow indicates direction of magnetic field that generates a positive output reading in normal measurement configuration.

<QMC6309H>

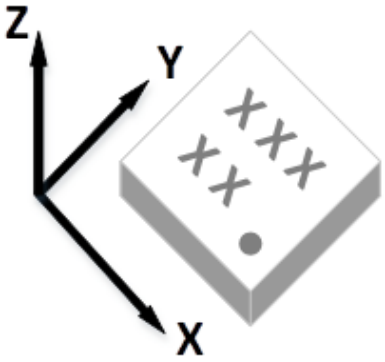


Figure 2. Package 3-D View

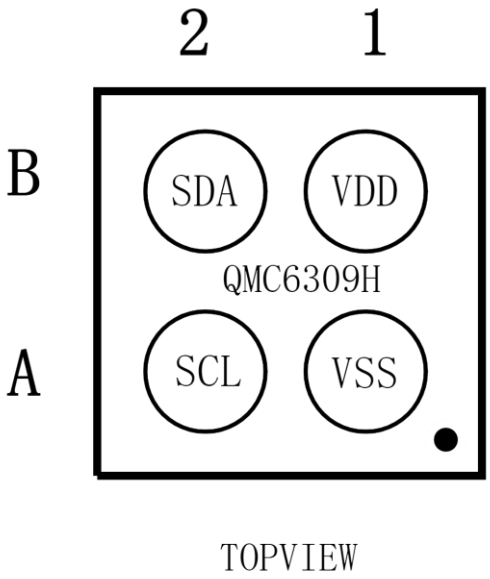


Figure 3. Package Top View

Table 5. Pin Configurations

PIN No.	PIN NAME	I/O	TYPE	Function
A1	VSS	-	-	Ground
A2	SCL	I	CMOS	I^3C/ I^2C serial clock line
B1	VDD	-	Power	Supply Voltage
B2	SDA	I/O	CMOS	I^3C/ I^2C serial data line

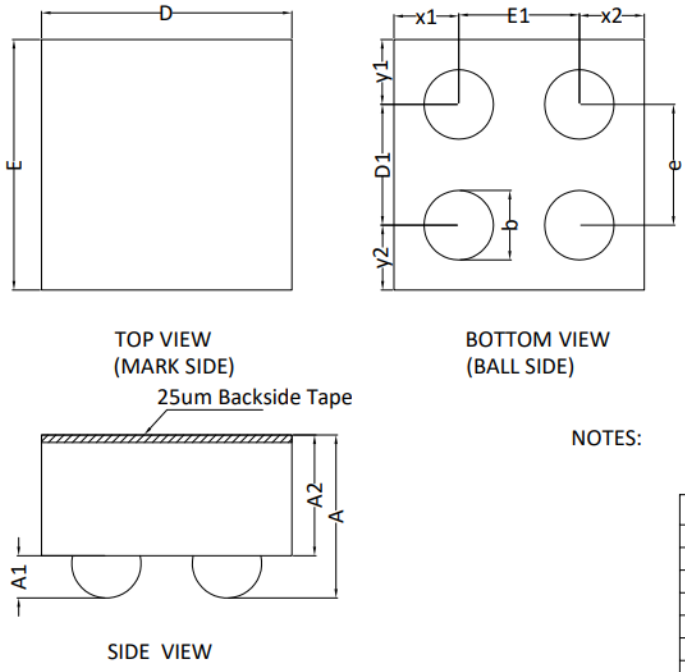
3.2 Package Outlines

3.2.1 Package Type

WLCSP

3.2.2 Package Size

0.8mm (Length)*0.8mm (Width)*0.5mm (Height)



NOTES:

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLMETER)

SYMBOL	MIN	NOM	MAX
A	0.500	0.540	0.580
A1	0.110	0.140	0.170
A2	0.375	0.400	0.425
D	0.770	0.790	0.810
E	0.770	0.790	0.810
D1		0.400BSC	
E1		0.400BSC	
e		0.400BSC	
b	0.200	0.230	0.260
x1		0.215REF	
x2		0.215REF	
y1		0.215REF	
y2		0.215REF	

Figure 4. Package Size

3.2.3 Marking

Tracking code: X1X2X3X4X5

X1X2X3X4= Package Lot
X5= Supplier code
●= Pin1 Identifier

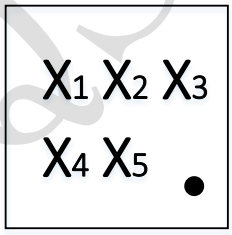


Figure 5. Chip Marking

4. EXTERNAL CONNECTION

4.1 Recommended External Connection

4.1.1 I²C Bus interface

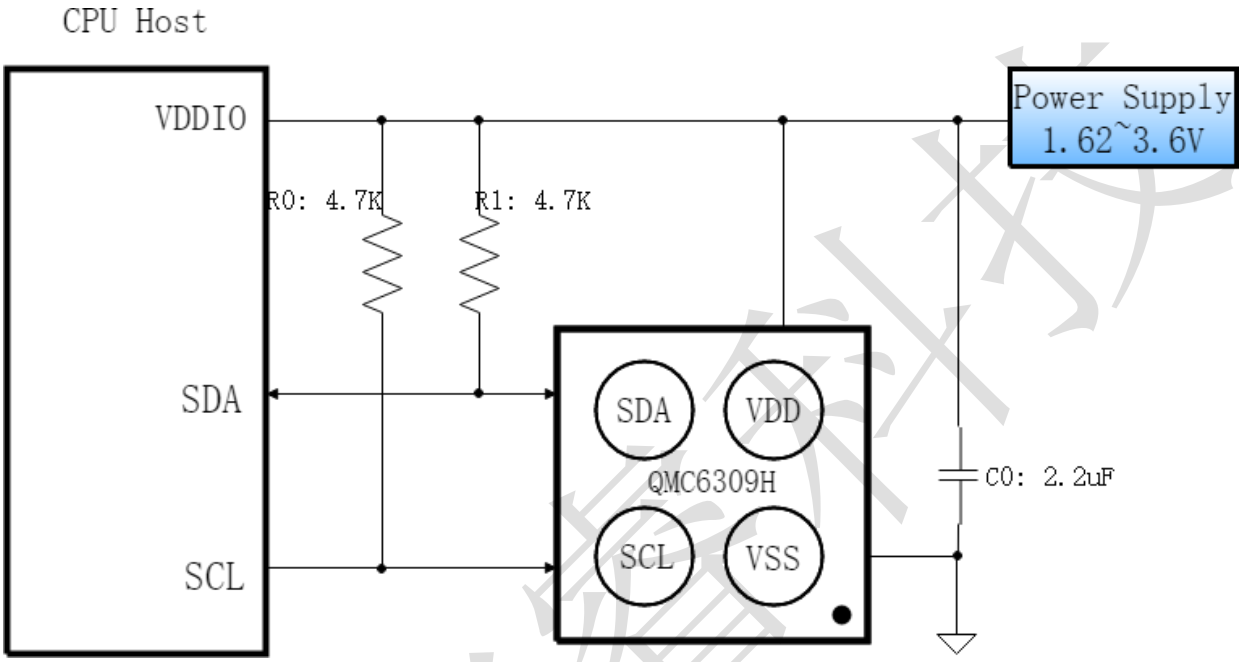


Figure 6. When VDDIO is the same as VDD

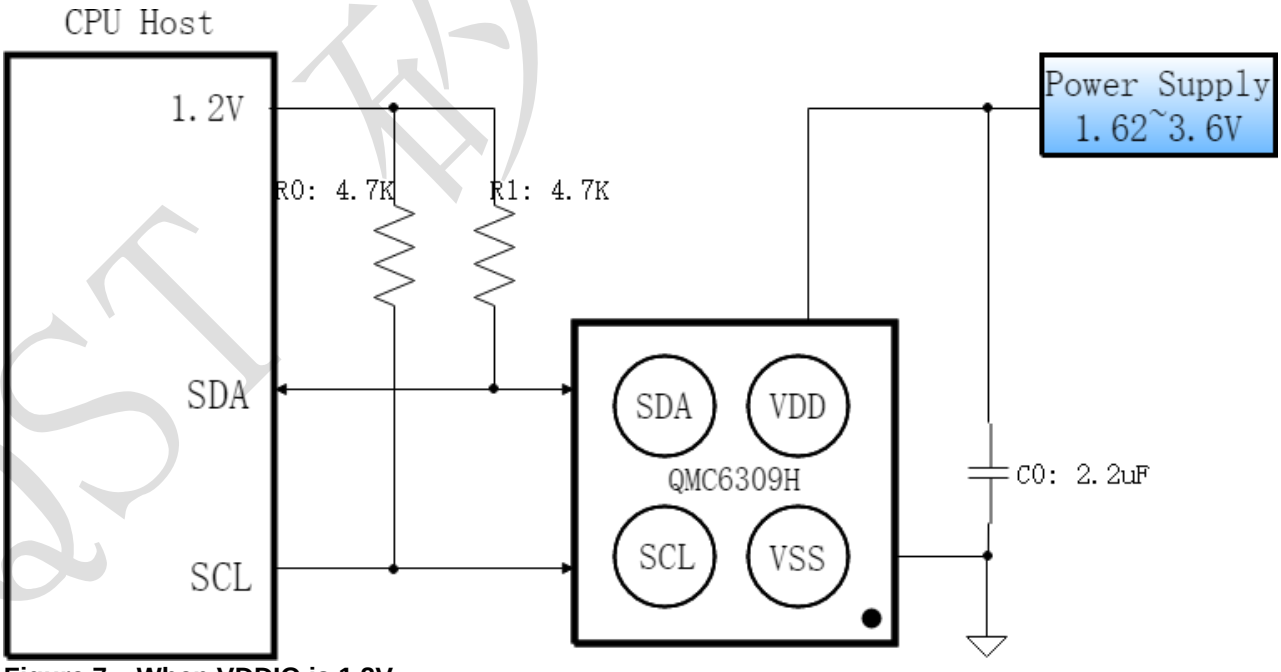


Figure 7. When VDDIO is 1.2V

4.1.2 I³C Bus interface

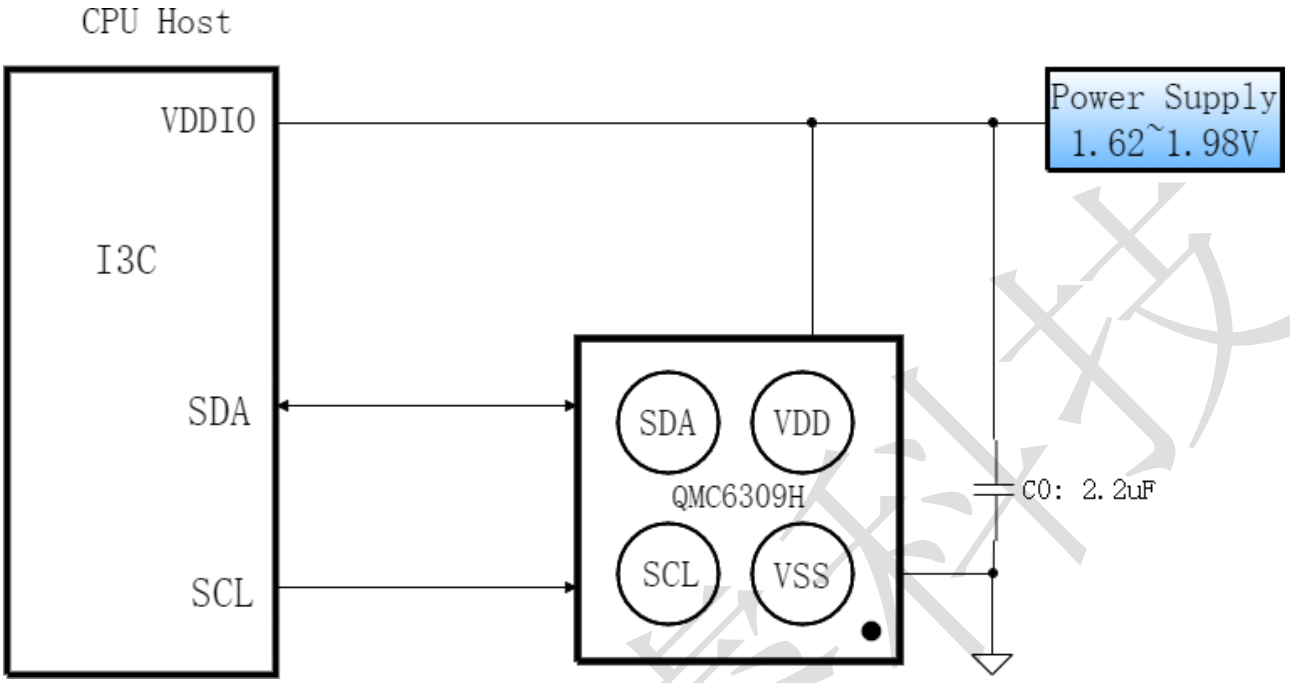


Figure 8. When VDDIO is the same as VDD

4.2 Mounting Considerations

The following is the recommend printed circuit board (PCB) footprint for the QMC6309H. Due to the fine pitch of the pads, the footprint should be properly centered in the PCB.

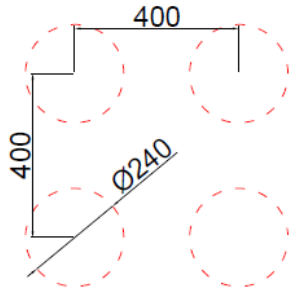


Figure 9. QMC6309H PCB footprint

4.3 Layout Considerations

Besides keeping all components that may contain ferrous materials (nickel, etc.) away from the sensor on both sides of the PCB, it is also recommended that there is no conducting copper line under/near the sensor in any of the PCB layers.

4.3.1 Solder Paste

A 4-mil stencil and 100% paste coverage is recommended for the electrical contact pads.

4.3.2 Reflow Assembly

This device is classified as MSL 1 with 260°C peak reflow temperature. Reference IPC/JEDEC standard J-STD-033 for additional information.

No special reflow profile is required for QMC6309H, which is compatible with lead eutectic and lead-free solder paste reflow profiles. QST recommends adopting solder paste manufacturer's guidelines. Hand soldering is not recommended.

4.3.3 External Capacitors

The external capacitors C0 should be ceramic type with low ESR characteristics. The exact ESR value is not critical, but values less than 200 milli-ohms are recommended. Reservoir capacitor C0 is nominally 2.2 µF in capacitance. Low ESR characteristics may not be in many small SMT ceramic capacitors (0402), so be prepared to up-size the capacitors (0201) to gain low ESR characteristics.

5. BASIC DEVICE OPERATION

5.1 Anisotropic Magneto-Resistive Sensors

QMC6309H magneto-resistive sensor circuit consists of tri-axial sensors and application specific support circuits to measure magnetic fields. With a DC power supply is applied to the sensor two terminals, the sensor converts any incident magnetic field in the sensitive axis directions to a differential voltage output.

The device has an offset cancellation function to eliminate sensor and ASIC offsets. It also applies a self-aligned magnetic field to restore magnetic state before each measurement to ensure high accuracy. Because of these features, the QMC6309H doesn't need to calibrate every time in most of application situations. It may need to be calibrated once in a new system or a system changes a new battery.

5.2 Power Management

There is only one power supply pin to the device. VDD provides power for all the internal analog and digital functional blocks and I/O.

When the device is powered on, all registers are reset by POR (Power-On-Reset), then the device transits to the suspend mode and waits for further commands.

Table 6 provides references for two power states.

Table 6: Power States

Power State	VDD	Power State description
1	0V	Device Off, No Power Consumption
2	1.62V~3.6V	Device On, Enters Suspend Mode after POR, waiting for further commands

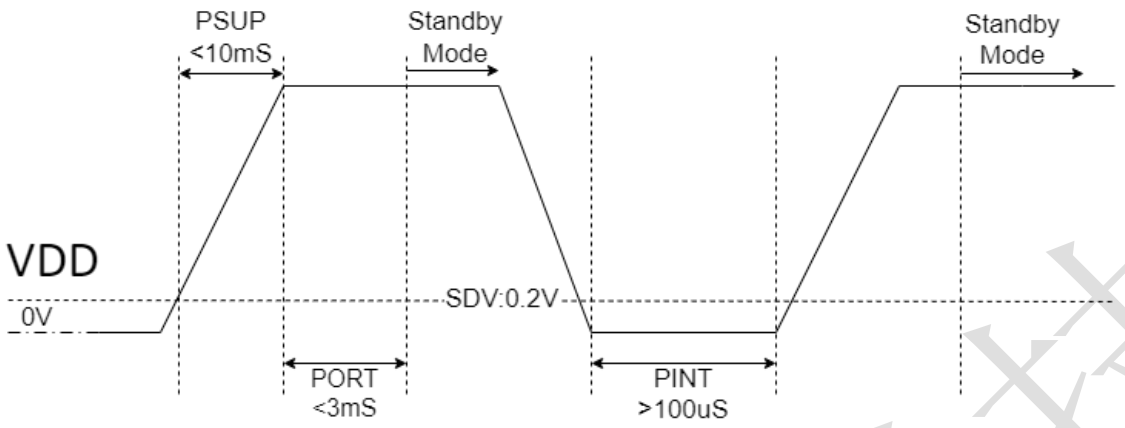
5.3 Power On/Off Time

After the device is powered on, some time periods are required for the device fully functional. The external power supply requires a time period for voltage to ramp up (PSUP), it is less than~10 milli-second. However, it isn't controlled by the device. The Power-On-Reset time period (PORT) includes time to reset all the logics, load values in NVM to proper registers, enter the standby mode and get ready for analogy measurements. The power on/off time related to the device is in Table 7.

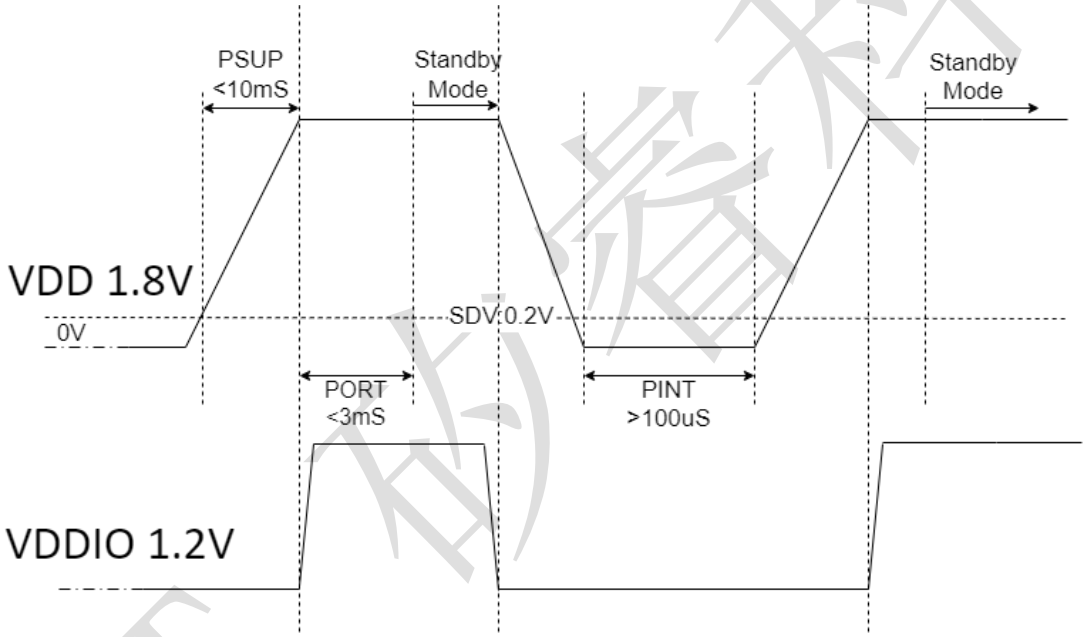
Table 7. Time Required for Power On/Off

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time[1]	PSUP	Time Period that VDD changes from 0.2V to Operating Voltage			10	mS
POR Completion Time[1]	PORT	Time Period After VDD at Operating Voltage to Ready for I^2C Command[2]			3	mS
Power off Voltage[1]	SDV	Voltage that Device Considered to be Power Down[2].			0.2	V
Power on Interval[1]	PINT	Time Period Required for Voltage Lower than SDV to Enable Next POR[2]	100			uS

Notes:
1. Reference value for design
2. When POR circuit detects the rise of VDD voltage, it resets internal circuits and initializes the registers. After reset, QMC6309H transits to Suspend Mode.



Power On/Off Timing
Single Power Supply



Power On/Off Timing
VDD=1.8V VDDIO=1.2V

Figure 10. Power On/Off Timing

Note: when VDD=1.8V/ VDDIO=1.2V, It is strongly recommended to power on VDD before VDDIO, and power off VDD after VDDIO.

5.4 Communication Bus Interface I²C and Its Addresses

This device will be connected to a serial interface bus as a slave device under the control of a master device, such as the processor. Control of this device is carried out via I²C.

This device is compliant with I²C Bus Specification. As an I²C compatible device, this device has a 7-bit serial address and supports I²C protocols. This device supports standard and fast speed modes, 100kHz and 400kHz, respectively. External pull-up resistors are required to support all these modes.

There is only one I²C address available. The default value is 0CH.

5.5 Internal Clock

This device has an internal clock for internal digital logic functions and timing management. This clock is not available to external usage.

5.6 Temperature Compensation

This device has a built-in Temperature sensor and Temperature compensation function. The compensated magnetic sensor data is placed in the Output Data Registers automatically.

5.7 FIFO

There are three operation modes of FIFO. The FIFO can be configured as FIFO mode, STREAM mode or BYPASS mode.

BYPASS mode (0X2E [7:6] = 0)
In BYPASS mode, only the current magnetic data of selected axes can be read out from the FIFO. The FIFO acts like the STREAM mode with a depth of 1. Compare to reading directly from data register, this mode has the advantage of ensuring the package of data are from same point of timeline. The data registers are updated sequentially and have chance for the data sampled in different time. Also, if any old data is discarded, FIFO_OR will be set to be logic 1, similar as that in stream mode.

FIFO mode (0X2E [7:6] = 1 or 3)
In FIFO mode, the magnetic data of selected axes are stored in the buffer memory. If enabled, FIFO_WTMK_INT will be set 1 when the buffer filled up to the defined level. buffer will continuously be filled until the fill level reaches 8. When the buffer is full, data collection stops, and the new data will be ignored. Also, FIFO_FULL_INT will be set 1.

STREAM mode (0X2E [7:6] = 2)
In STREAM mode, the magnetic data of selected axes will be stored into the buffer until the buffer is full. The buffer's depth is 8 now. When the buffer is full, data collection continues, and the oldest data is over-written. If enabled, FIFO_WTMK_INT will be set 1 when the fill level reached to the defined level. Also, when buffer is full, FIFO_FULL_INT will be set 1. If any old data is discarded, the FIFO_OR will be set to be logic 1.

FIFO_CHNL_SEL (0X2E [2:0])
User can select data of certain axis to be stored in the FIFO. This configuration can be done by setting FIFO_CHNL_SEL, where '111b' for x-, y-, z-axis, '001b' for x-axis only, '010b' for y-axis only, '100b' for z-axis only.

If all the 3 axes data are selected, the format of data read from 0x2F is as follows:

XLSB	XMSB	YLSB	YMSB	ZLSB	ZMSB

These comprise one frame.

If only one axis is enabled, the format of data read from 0x2F is as follows:

YLSB	YMSB

These comprise one frame.
If the frame is not read completely, the remaining parts of the frame will be discarded.

FIFO_FRAME_CNT (0X20 [7:4])
This register is used for recording how much data is stored in FIFO memory. The range is 0~8.

FIFO_FULL_INT (0X20 [0])
This flag is triggered when the buffer has been fully filled. In FIFO mode (FIFO_MODE = 1 or 3) or STREAM mode (FIFO_MODE = 2), the fill level is 8, in BYPASS mode (FIFO_MODE = 0) the fill level is 1.

FIFO_WTMK_INT (0X20 [1])

This flag is triggered when the level of buffer reached the level defined by register FIFO_WTMK (0x2E<5:3>). When FIFO_FRAME_CNT >= FIFO_WTMK, the flag will be set to 1. And the flag will be set to 0 if FIFO_FRAME_CNT is less than FIFO_WTMK.

FIFO_OR _INT (0X20 [2])
This flag is triggered when FIFO is full and additional data is written into FIFO. This FIFO_OR _INT can be considered as flag of discarding old data.

6. MODES OF OPERATION

6.1 Modes Transition

The device has three different modes, controlled by register (0x0A), mode bits Mode[1:0]. The main purpose of these modes is for power management. The modes can be transited from one to another, as shown below, through I²C commands of changing mode bits. The default mode is Suspend Mode.

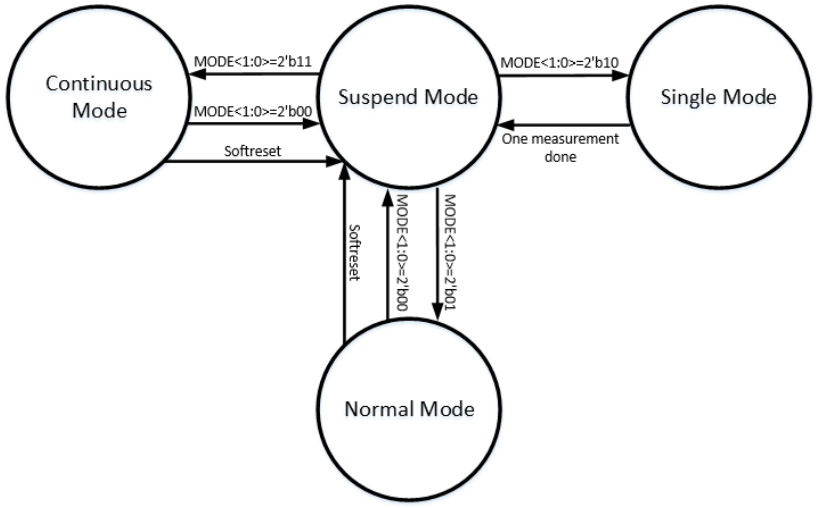


Figure 11. Modes Transition

6.2 Description of Modes

6.2.1 Normal Mode

During the Normal mode (MODE bits= 2'b01), the magnetic sensor continuously makes measurements and places measured data in data output registers. The field range register is controlled by RNG<1:0> in register 0BH and data output rate is controlled by ODR<1:0> in register 0AH. They should be set up properly for your applications in the normal mode.

6.2.2 Single Mode

During the Single Mode (MODE bits=2'b10), the whole chip runs only once and enter in the suspend mode after 1 measurement is finished.

6.2.3 Continuous Mode

During the Continuous Mode (MODE bits=2'b11), the whole chip runs all the time without sleep time, so the maximum ODR can be got at this mode.

6.2.4 Suspend Mode

Suspend mode is the default magnetometer state upon POR and soft reset. Only few function blocks are activated in this mode which keeps power consumption as low as possible. In this state, register values are hold on by a lower power LDO, I³C / I²Css interface is active, and all register read and write are allowed. There is no magnetometer measurement in this Mode.

7. APPLICATION EXAMPLES

7.1 Normal Mode Setup Example

(1) Write Register 0BH by 0x40 (Define Set/Reset mode, with Set/Reset On, Field Range 32Guass, ODR=200HZ)

(2) Write Register 0AH by 0x65 (Set Normal Mode, OSR1=8, OSR2=8)

7.2 Continuous Mode Setup Example

(1) Write Register 0BH by 0x00 (Define Set/Reset mode, with Set/Reset On, Field Range 32Guass)

(2) Write Register 0AH by 0x67 (Set Continuous Mode, OSR1=8, OSR2=8)

7.3 Self-test Example

(1) Write Register 0AH by 0x00 (Set Suspend Mode)

(2) Write Register 0BH by 0x00

(3) Write Register 0AH by 0x03 (Set Continuous Mode)

(4) Waiting 20 millisecond

(5) Write Register 0EH by 0x80 (Set Self-test enable)

(6) Loop to check status register 09H[2] until measurement ends, ”1” means ready

(7) Read data Register 13H ~ 15H

(8) Self-test Judgment: If the delta value of each axis is in the range of following table, the chip is working properly.

	Self-test X(13H)	Self-test Y(14H)	Self-test Z(15H)
Criteria (Unit: LSB)	-50 ~ -1	-50 ~ -1	-50 ~ -1

7.4 Suspend Mode Example

(1) Write Register 0AH by 0x00

7.5 Measurement Example

(1) Check status register 09H [0], “1” means data is ready

(2) Read data register 01H ~ 06H

7.6 Soft Reset Example

(1) Write Register 0BH by 0x80

(2) Write Register 0BH by 0x00

8. I3C COMMUNICATION PROTOCOL

I3C bus of QMC6309H supports I2C mode(400KHz) and I3C SDR mode(12.5MHz).

8.1 I2C Mode

After power-on, QMC6309H communicates as I2C slave until I3C Dynamic Address is assigned.

8.1.1 I2C Timings

Below table and graph describe the I2C communication protocol times

Table 8. I2C Timings

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL Clock	f_{scl}	0	100	400	kHz
SCL Low Period	t_{low}	1.3			uS
SCL High Period	t_{high}	0.6			μS
SDA Setup Time	t_{sudat}	0.1			μS
SDA Hold Time	t_{hddat}	-		-	μS
Start Hold Time	t_{hdsta}	0.6			μS
Start Setup Time	t_{susta}	0.6			μS
Stop Setup Time	t_{susto}	0.6			μS
New Transmission Time	t_{buf}	1.3			μS
Rise Time	t_r (t_{rcl},t_{rdat})	0.02		0.3	μS
Fall Time	t_f (t_{fcl},t_{fdat})	0.02		0.3	μS

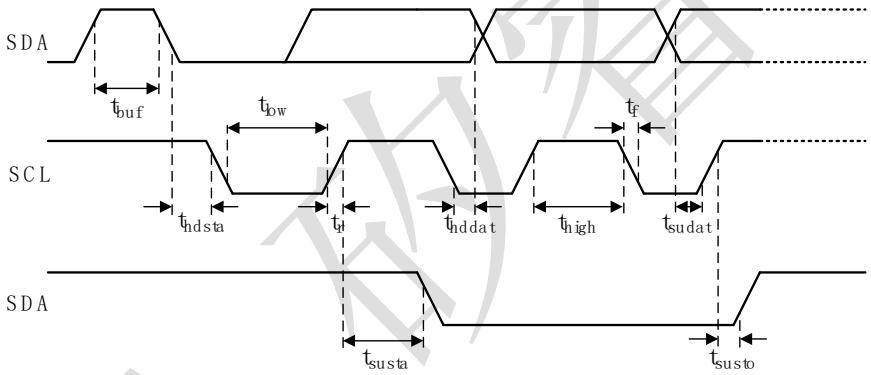


Figure 12. I2C Timing Diagram

8.1.2 I2C R/W Operation

8.1.2.1 Abbreviation

Table 9. Abbreviation

SACK	Acknowledged by slave
MACK	Acknowledged by master
NACK	Not acknowledged by master
RW	Read/Write

8.1.2.2 Start/Stop/Ack

START: Data transmission begins with a high to transition on SDA while SCL is held high. Once I2C transmission starts, the bus is considered busy.
STOP: STOP condition is a low to high transition on SDA line while SCL is held high.

ACK: Each byte of data transferred must be acknowledged. The transmitter must release the SDA line during the acknowledge pulse while the receiver must then pull the SDA line low so that it remains stable low during the high period of the acknowledge clock cycle.
NACK: If the receiver doesn't pull down the SDA line during the high period of the acknowledge clock cycle, it's recognized as NACK by the transmitter.

8.1.2.3 I²C Write

I²C write sequence begins with start condition generated by master followed by 7 bits slave address and a write bit (R/W=0). The slave sends an acknowledge bit (ACK=0) and releases the bus. The master sends the one-byte register address. The slave again acknowledges the transmission and waits for 8 bits data which shall be written to the specified register address. After the slave acknowledges the data byte, the master generates a stop signal and terminates the writing protocol.

Table 10. I²C Write

START	Slave Address							R W	SACK	Register Address (0x0A)								SACK	Data (0x01)								SACK	STOP
	0	0	0	1	1	0	0	0		0	0	0	0	1	0	1	0		0	0	0	0	0	0	0	1		

8.1.2.4 I²C Read

I²C read sequence consists of a one-byte I²C write phase followed by the I²C read phase. A start condition must be generated between two phases. The I²C write phase addresses the slave and sends the register address to be read. After slave acknowledges the transmission, the master generates again a start condition and sends the slave address together with a read bit (R/W=1). Then master releases the bus and waits for the data bytes to be read out from slave. After each data byte, the master has to generate an acknowledge bit (ACK = 0) to enable further data transfer. A NACK from the master stops the data being transferred from the slave. The slave releases the bus so that the master can generate a STOP condition and terminate the transmission.

Table 11. I²C Read

START	Slave Address							R W	SACK	Register Address (0x00)								SACK		
	0	0	0	1	1	0	0	0		0	0	0	0	0	0	0	0			
START	Slave Address							R W	SACK	Data (0x00)								NACK	STOP	
	0	0	0	1	1	0	0	1		0	0	0	0	0	0	0	0			

8.2 I³C Mode

I³C bus is compliant with Open-Drain mode and Push-Pull mode. Open-Drain/Push-Pull mode is selected automatically by I³C function.

8.2.1 I³C Open-Drain/Push-Pull mode timing

Table 12. Open-drain mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock "High" time	tHIGH			41	ns
SCL clock "High" time	tLOW_OD	200			ns
SDA fall time	tSU_OD			12	ns
SDA setup time	tfDA_OD	3			ns
START Condition hold time	tCAS	38.4			ns
STOP Condition set time	tCBP	19.2			ns
Bua available condition	tAVAL	1			ns

Bus idle condition	tIDLE	1			ns

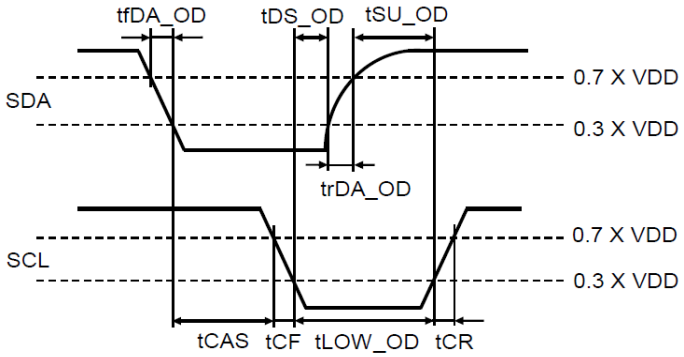


Figure 13. START condition timing (Open-drain mode)

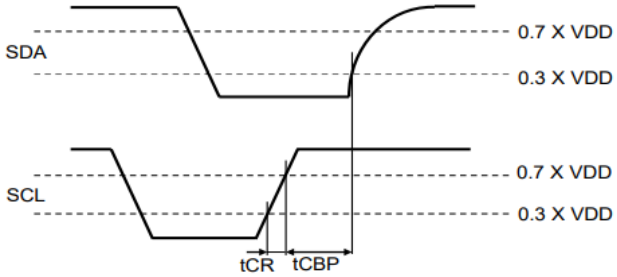


Figure 14. STOP condition timing (Open-drain mode)

Table 13. Push-Pull mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL	0.01	12.6	12.9	MHz
SCL clock “High” time	tHIGH	24.0			ns
SCL clock “Low” time	tLOW_OD	24.0			ns
Clock in to Data Out	tSCO			12.0	ns
SCL rise time	tCR			150*1/fSCL	ns
SCL fall time	tCF			150*1/fSCL	ns
SDA setup time	tfDA_OD	3			ns
Capacitive Load per Bus Line(SDA/SCL)	Cb			50	pF

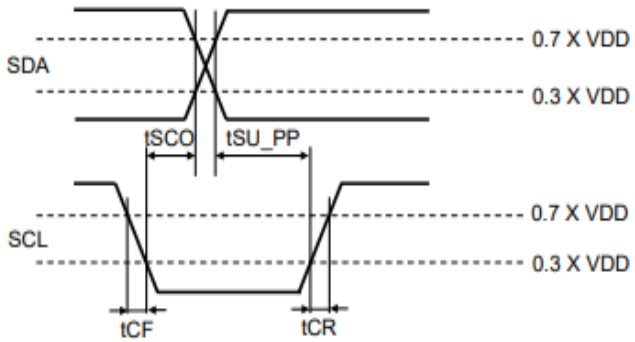


Figure 15. Data Output timing(Push-Pull mode)

8.2.2 Bus Protocol Configuration

Table 14.

Protocol	Bit length	Description	Abbreviation
START condition	-	Input at the start of communication	S
Slave Address	7	Select Slave Device	-
Read/Write control bit	1	0: write 1: read	R/W
Register Address	8	Set access address	-
Control data	8	Write/Read data	-
Repeated START	-	Two or more instance of a START in a row without an intervening STOP	Sr
STOP condition	-	Input at the end of communication	P
Acknowledge	-	Generated when receiving data	ACK
Transition Bit	-	Generated when sending data	T
Parity Bit	-	Received when writing data	PAR
HDR Exit Pattern	-	Entered when returning from error condition	-

8.2.2.1. START/STOP Condition

If the SDA line is driven to “Low” from “High” when the SCL line is “High”, a START condition is generated. Every instruction starts with a START condition.

If the SDA line is driven to “High” from “Low” when the SCL line is “High”, a STOP condition is generated. Every instruction stops with a STOP condition.

The I^3C START and STOP are identical to the I^2C START and STOP in their signaling, but they may vary from I^2C in their timing.

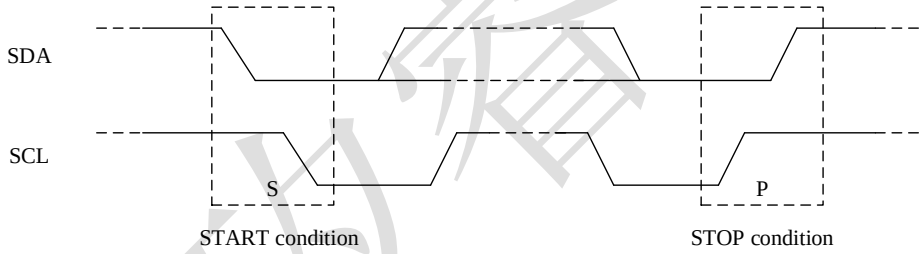


Figure 16. START and STOP condition

8.2.2.2 Acknowledge

The IC that is transmitting data releases the SDA line (in the “High” state) after sending 1-byte data. The IC that receives the data drives the SDA line to “Low” on the next clock pulse. This operation is referred as acknowledge. With this operation, whether data has been transferred successfully can be checked.

In I^2C mode, QMC6309H generates an acknowledge after reception of a START condition and Slave Address. When a WRITE instruction is executed, QMC6309H generates an acknowledge (without Handoff) after every byte is received. When a READ instruction is executed, QMC6309H generates an acknowledge (without Handoff) then transfers the data stored at the specified address. Next, QMC6309H releases the SDA line then monitors the SDA line. If a Master generates an acknowledge instead of a STOP condition, QMC6309H transmits the 8 bits data stored at the next address. If no acknowledge is generated, QMC6309H stops data transmission.

QMC6309H generates an acknowledge after reception of a START condition and Broadcast Address (7’h7E). When a WRITE instruction is executed, QMC6309H generates an acknowledge (with Handoff). When a READ instruction is executed, QMC6309H generates an acknowledge (without Handoff).

.

In I^3C SDR mode, QMC6309H generates an acknowledge after reception of a START condition and under following conditions.

(1) When receiving its own Dynamic Address.

(2) When a Broadcast Address is received.

(3) When a Slave Address is received by Dynamic Address Assignment.

In case of (1), when the R/W bit is set to “1”, it returns one clock (without Handoff), and when R/W bit is set to “0”, it returns an acknowledge of half clock (with Handoff). In case of (2), when the R/W bit is set to “0”, it returns an acknowledge of half clock (with Handoff). In case of (3), it returns an acknowledge of one clock (without Handoff).

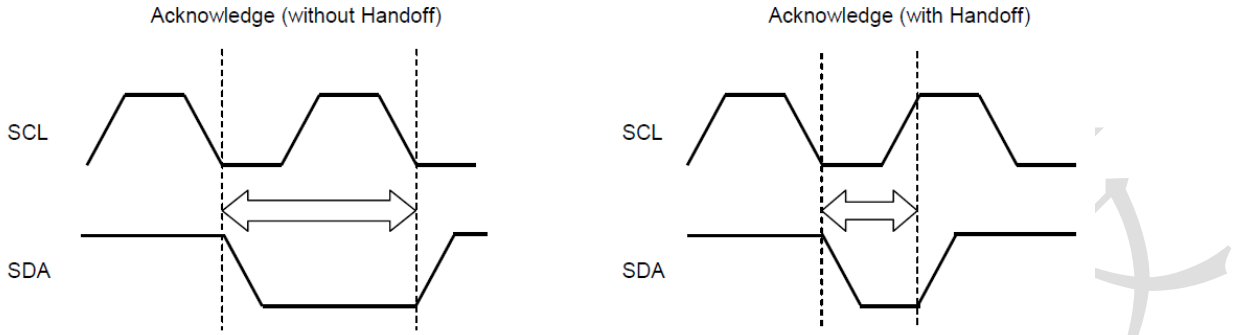


Figure 17. Generation of Acknowledge

8.2.2.3 Transition-Bit (T-Bit)

In I3C, the data words match I2C only in the sense that they are both 9 bits long.
In I2C, the ninth data bit written by the Master is an acknowledge by the Slave. By contrast, in I3C the ninth data bit written by the Master is the parity of the preceding eight data bits. In SDR terms, the ninth bit of write data is referred to as the T-Bit (for ‘Transition’). The ninth data bit of each SDR data word written by the I3C Master (also referred to as the T-Bit) is a Parity bit, calculated using odd parity. Parity can help in detecting noise-caused errors on the line. The value of this parity bit shall be the XOR of the 8 data bits with 1, i.e.: XOR(Data [7:0], 1).
T (Parity) bit writes shall always be kept valid through the SCL high period. In the case of a T-Bit representing the last data byte, the write is therefore kept valid through the SCL high period, and the next SCL low can then be used to either change the SDA, or not change the SDA, in preparation for the Repeated START condition or STOP condition that follows.
If parity is different, QMC6309H will not receive data.
In I2C, the ninth data bit from Slave to Master is an acknowledge by the Master. By contrast, in I3C this bit allows the Slave to end a read and allows the Master to abort a read. In SDR terms, the ninth bit of read data is referred to as the T-Bit (for ‘Transition’).
If transmission of the number of bytes set by SETMRL has not been completed, QMC6309H generates.
T-Bit = “1” and transmits data at the next address from the falling edge of SCL after that. When transmission of the number of bytes set by SETMRL is completed, QMC6309H generates T-Bit = “0” and then releases the SDA line.

8.2.2.4 Slave Address

The Slave Address of QMC6309H is 7’h0C
When a Slave Address is transferred, the IC whose device address matches the transferred Slave Address generates an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit.
When the R/W bit is set to “1”, READ instruction is executed. When the R/W bit is set to “0”, WRITE instruction is executed.

8.2.2.5 Broadcast Address

The Broadcast Address of Slave devices is 7’h7E. All I3C Slaves match address value 7’h7E. No I2C Slave will match address 7’h7E.The first byte including a Broadcast Address is transmitted after a START condition, and all I3C Slaves are selected on the bus.
When a Broadcast Address is transferred, all I3C Slaves generate an acknowledge then executes an instruction. The 8th bit (least significant bit) of the first byte is a R/W bit. When the R/W bit is set to “1”, READ instruction is executed. When the R/W bit is set to “0”, WRITE instruction is executed.

8.2.2.6 Dynamic Address

In I2C mode, QMC6309H is assigned a Dynamic Address by performing SETDASA or ENTDAA flow. After the flow is completed, QMC6309H communicates in I3C SDR mode.

8.2.2.7 SETDASA (Set Dynamic Address from Static Address)

The SETDASA CCC is a flow for assigning Dynamic Address based on the Slave Address in the I²C state. QMC6309H can assign a Dynamic Address by Direct CCC. The Slave Address of QMC6309H is 7'h0C.
The newly assigned address is transmitted in the Dynamic Address byte shown below, where the 7 most significant bits (Bits [7:1]) contain the 7-bit Dynamic Address, and the least significant bit (Bit [0]) is filled with the value 1'b0. If this least significant bit (Bit [0]) has the value 1'b1, QMC6309H will not accept the Dynamic Address.

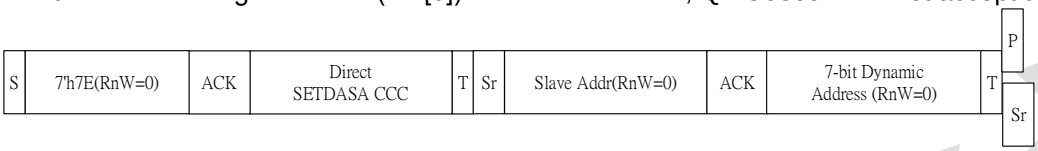


Figure 18. SETDASA Format

8.2.2.8 ENTDAA (Enter Dynamic Address Assignment)

The ENTDAA CCC is a flow for assigning Dynamic Address based on the 48-bit Provisional ID (PID), Bus Characteristic Register (BCR) and Device Characteristic Register (DCR). Data input will follow in the flow of Figure 19, The values of QMC6309H are PID = 48'h000012345678, BCR = 8'h07, DCR = 8'h43.

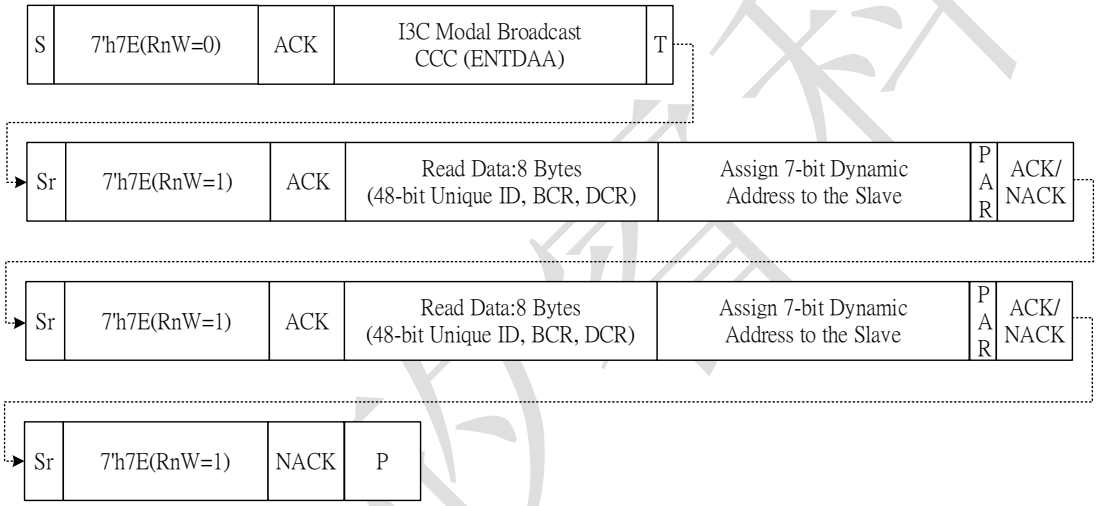


Figure 19. ENTDAA Format

8.2.3 I³C SDR Mode

When Dynamic Address is assigned properly, QMC6309H shifts to I³C SDR mode. I³C SDR mode is significantly similar to the I²C protocol in terms of procedures and conditions. In I³C SDR mode, QMC6309H can communicate with Private Messages or Common Command Code (CCC).

8.2.3.1 Private Messages

8.2.3.1.1 Write Instruction

When the R/W bit is set to "0", QMC6309H performs write operation. In write operation, QMC6309H generates an acknowledge (with Handoff) after receiving a START condition and the first byte (Dynamic Address). The second byte is used to specify the address of an internal control register and is based on the MSB-first configuration. After receiving the second byte (register address), QMC6309H receives a T-Bit then receives the third byte.
The third and the following bytes represent control data. Control data consists of 8 bits and is based on the MSB-first configuration. QMC6309H generates a T-Bit after every byte is received. Data transfer always stops with a STOP condition generated by the Master. QMC6309H can write multiple bytes of data at a time. The maximum value is determined Max Write Length.

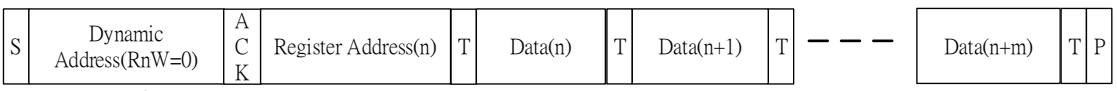


Figure 20. I³C Wirte Format

8.2.3.1.2 Read Instruction

When the R/W bit is set to “1”, QMC6309H performs read operation. The read operation requires to execute WRITE instruction as dummy before a Slave Address for the READ instruction (R/W bit = “1”) is transmitted. In read operation, a START condition is first generated then a Dynamic Address for the WRITE instruction (R/W bit = “0”) and a read address are transmitted sequentially. After QMC6309H receives a T-Bit in response to this address transmission, a Repeated START condition and a Dynamic Address for the READ instruction (R/W bit = “1”) are generated again. QMC6309H generates a T-Bit in response to this Dynamic Address transmission. Next, QMC6309H transfers the data at the specified address then increments the internal address counter by one. If the Master generates a STOP condition instead of an acknowledge after data is transferred, the read operation stops.

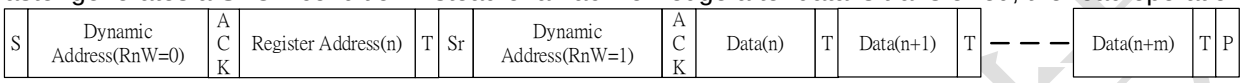


Figure 21. I³C Read Format

8.2.3.1.3 Common Command Code(CCC)

QMC6309H supports some Common Command Codes(CCCs) defined in the specification of I³C.

8.2.3.1.3.1 Broadcast CCC

All Slaves inspect every received Broadcast command, even if the Slave doesn’t support and ignore the Broadcast command.

Table 15. CCC (Broadcast)

Command code	Command Name	Broadcast/Direct	Set/Get	Brief Description
00h	ENEC	Broadcast	Set	Enable Events Command,”1”: enable
01h	DISEC	Broadcast	Set	Disable Events Command,”1”: disable
02h	ENTAS0	Broadcast	Set	Enter Activity State 0
03h	ENTAS1	Broadcast	Set	Enter Activity State 1
04h	ENTAS2	Broadcast	Set	Enter Activity State 2
05h	ENTAS3	Broadcast	Set	Enter Activity State 3
06h	RSTDAA	Broadcast	Set	Reset Dynamic Address Assignment
07h	ENTDAA1	Broadcast	Get	PID [47:40]
	ENTDAA2	Broadcast	Get	PID [39:32]
	ENTDAA3	Broadcast	Get	PID [31:24]
	ENTDAA4	Broadcast	Get	PID [23:16]
	ENTDAA5	Broadcast	Get	PID [15:8]
	ENTDAA6	Broadcast	Get	PID [7:0]
	ENTDAA7	Broadcast	Get	BCR
	ENTDAA8	Broadcast	Get	DCR
	ENTDAA9	Broadcast	Set	Enter Dynamic Address
08h	DEFSLVS	Broadcast	-	Not supported
09h	SETMWL1	Broadcast	Set	Max Write Length [15:8]
	SETMWL2	Broadcast	Set	Max Write Length [7:0]
0Ah	SETMRL1	Broadcast	Set	Max Read Length [15:8]
	SETMRL2	Broadcast	Set	Max Read Length [7:0]
0Bh	ENTTM	Broadcast	-	Not supported
0Ch-1Fh	Reserved			
20h	ENTHDR0	Broadcast	-	Not supported
21h	ENTHDR1	Broadcast	-	
22h	ENTHDR2	Broadcast	-	
23h	ENTHDR3	Broadcast	-	
24h	ENTHDR4	Broadcast	-	
25h	ENTHDR5	Broadcast	-	
26h	ENTHDR6	Broadcast	-	
27h	ENTHDR7	Broadcast	-	

28h	SETXTIME1	Broadcast	-	
	SETXTIME2	Broadcast	-	
	SETXTIME3	Broadcast	-	
	SETXTIME4	Broadcast	-	
	SETXTIME5	Broadcast	-	
	SETXTIME6	Broadcast	-	
29h-7Fh	Reserved			

8.2.3.1.3.2 Direct CCC

A Direct CCC is directed to one or more specific I^{3}C Slaves, selected by the Slave Dynamic Address. Every Direct CCC Command ends with a STOP or a Repeated START, followed by the I^{3}C Broadcast Address (7'h7E).

Table 16. CCC (Direct)

Command code	Command Name	Broadcast/Direct	Set/Get	Brief Description
80h	ENEC	Direct	Set	Enable Events Command,"1": enable
81h	DISEC	Direct	Set	Disable Events Command,"1": disable
82h	ENTAS0	Direct	Set	Enter Activity State 0
83h	ENTAS1	Direct	Set	Enter Activity State 1
84h	ENTAS2	Direct	Set	Enter Activity State 2
85h	ENTAS3	Direct	Set	Enter Activity State 3
86h	RSTDAA	Direct	Set	Reset Dynamic Address Assignment
87h	SETDASA	Direct	Set	Set Dynamic Address
88h	SETNEWDA	Direct	Set	Set new Dynamic Address
89h	SETMWL1	Direct	Set	Max Write Length [15:8]
	SETMWL2	Direct	Set	Max Write Length [7:0]
8Ah	SETMRL1	Direct	Set	Max Write Length [15:8]
	SETMRL2	Direct	Set	Max Write Length [7:0]
8Bh	GETMWL1	Direct	Get	Not supported
	GETMWL2	Direct	Get	Not supported
8Ch	GETMRL1	Direct	Get	Not supported
	GETMRL2	Direct	Get	Not supported
8Dh	GETPID1	Direct	Get	PID [47:40]
	GETPID2	Direct	Get	PID [39:32]
	GETPID3	Direct	Get	PID [31:24]
	GETPID4	Direct	Get	PID [23:16]
	GETPID5	Direct	Get	PID [15:8]
	GETPID6	Direct	Get	PID [7:0]
8Eh	GETBCR	Direct	Get	BCR
8Fh	GETDCR	Direct	Get	DCR
90h	GETSTATUS1	Direct	Get	STATUS [15:8]
	GETSTATUS2	Direct	Get	STATUS [7:0]
91h	GETACCMST	Direct	-	Not supported
92h	Reserved			
93h	SETBRGTGT	Direct	-	Not supported
94h	GETMXDS	Direct	-	Not supported
95h	GETHDRCAP	Direct	Get	Not supported
96h-97h	Reserved			
98h	SETXTIME	Direct	-	Not supported
99h	SETYTIME	Direct	-	Not supported
9Ah-FFh	Reserved			

8.2.3.2 HDR Exit Pattern

The HDR Exit Pattern is defined thus:

- SDA starts High, SCL starts Low
- SDA falls (from High to Low) 4 times, while SCL remains Low for the whole time
- Each SDA transition is separated by a time interval of at least t_{DIG_H}
- A normal I³C STOP (SCL being High while SDA rises) always follows the HDR Exit Pattern, as shown below.

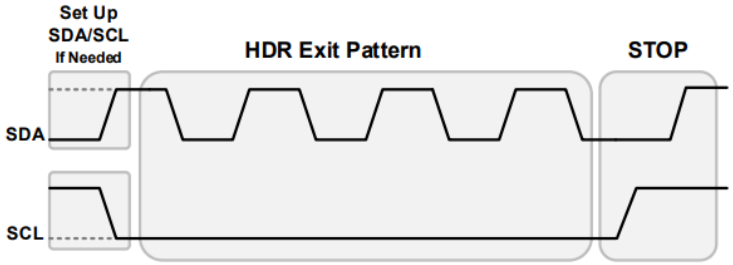


Figure 22. HDR Exit Pattern

8.2.4 In Band Interrupt(IBI)

QMC6309H supports In-Band Interrupt (IBI) using the SDA line
There are 5 signals used as IBI sources, data ready, self-test ready, data overflow, FIFO full and FIFO water mark. Whenever one of these interrupt sources is asserted and IBI is enabled, IBI controller would initiate an IBI by driving SDA line low and generating a START condition.
After QMC6309H generates a START condition, QMC6309H sends its own Dynamic Address and R/W bit="1" in Open-Drain. QMC6309H receives an acknowledgement from the Master and completes the IBI.

If there's any bus traffic during bus availability check period, IBI controller would respect that and try to initiate IBI after that communication is done. QMC6309H repeats until IBI is completed.

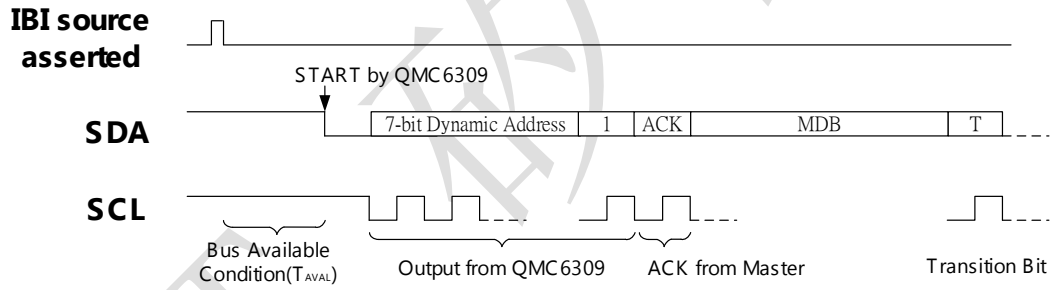


Figure 23. In-Band Interrupt Data format

9. REGISTERS

9.1 Register Map

The table below provides a list of the 8-bit registers embedded in the device and their respective function and addresses.

Chip ID is located at the address 00H, the default value is 90H. It can be used to recognize device.

Table 17. Register Map

Addr.	D7	D6	D5	D4	D3	D2	D1	D0	Access	POR /Soft Reset
00H	Chip ID								R Only	90H
01H	Data Output X LSB Register XOUT[7:0]								R Only	00H
02H	Data Output X MSB Register XOUT[15:8]								R Only	00H
03H	Data Output Y LSB Register YOUT[7:0]								R Only	00H
04H	Data Output Y MSB Register YOUT[15:8]								R Only	00H
05H	Data Output Z LSB Register ZOUT[7:0]								R Only	00H
06H	Data Output Z MSB Register ZOUT[15:8]								R Only	00H
09H	-	-	-	NVM_LOAD	NVM_RDY	ST_RDY	OVFL	DRDY	R Only	18H
0AH	OSR2[2:0]			OSR1[1:0]		-	MODE[1:0]		R/W	00H
0BH	SOFT_RST	ODR[2:0]			RNG[1:0]		SET/RESET MODE[1:0]		R/W	00H
0EH	SELF TEST	-	-	-	-	-	-	-	R/W	00H
13H	Data Output X Self-Test Register [7:0]								R Only	00H
14H	Data Output Y Self-Test Register [7:0]								R Only	00H
15H	Data Output Z Self-Test Register [7:0]								R Only	00H
20H	FIFO_FRAME_CNT[3:0]				-	FIFO_OR	FIFO_WM_INT	FIFO_FULL_INT	R Only	00H
21H				FF_WM_IEN	FF_FULL_IEN	ST_RDY_IEN	OVFL_IEN	DRDY_IEN	R/W	00H
2EH	FIFO_MODE [1:0]	FIFO_WTMK[2:0]				FIFO_CHNL_SEL[2:0]			R/W	00H
2FH	FIFO_DATA[7:0]								R Only	00H

9.2 Register Definition

9.2.1 Output Data Register

Registers 01H ~ 06H store the measurement data from each axis magnetic sensor in each working mode. In the normal mode, the output data is refreshed periodically based on the data update rate ODR setup in control registers 0AH. The data stays the same, regardless of reading status through I^2C, until new data replaces them. Each axis has 16-bit data width in 2's complement, i.e., MSB of 02H/04H/06H indicates the sign of each axis. The output data of each channel saturates at -32768 and 32767.

Register 13H~15H store the X,Y and Z self-test data under self-test mode separately. The self-test data of each channel

Register 2FH stores the FIFO data.

Table 18. Output Data Register

Addr.	7	6	5	4	3	2	1	0
01H	Data Output X LSB Register XOUT[7:0]							
02H	Data Output X MSB Register XOUT[15:8]							
03H	Data Output Y LSB Register YOUT[7:0]							
04H	Data Output Y MSB Register YOUT[15:8]							
05H	Data Output Z LSB Register ZOUT[7:0]							
06H	Data Output Z MSB Register ZOUT[15:8]							
13H	Selftest Output X Register XST[7:0]							
14H	Selftest Output Y Register YST[7:0]							
15H	Selftest Output Z Register ZST[7:0]							
2FH	FIFO_DATA[7:0]							

9.2.2 Status Registers1

There is one status register located in address 09H.
Register 09H has five bits indicating for status flags, the rest are reserved for factory use. The status registers are read only bits.

Table 19. Status Registers1

Addr.	7	6	5	4	3	2	1	0
09H	-	-	-	NVM_LOAD_DONE	NVM_RDY	ST_RDY	OVFL	DRDY

DRDY bit denotes the status of data, which is set when all three-axis data is ready and loaded to the output data registers in each mode. It is reset to “0” by reading the status register through I2C commands
DRDY: “0”: no new data, “1”: new data is ready

OVFL bit is set high when either axis code output exceeds the range of [-32000,32000] LSB and reset to “0” after the status register is read.
OVFL: “0”: no data overflow occurs; “1”: data overflow occurs.

ST_RDY denotes the status of built-in self-test measurement
ST_RDY: “0”: self-test not done yet; “1”: self-test is done, self-test data is ready for reading

NVM_RDY denotes the status of built-in Non-volatile Memory
NVM_RDY: “0”: NVM not ready for access; “1”: NVM ready for access

NVM_LOAD_DONE denotes the status of data loading from built-in Non-volatile Memory
NVM_LOAD_DONE: “0”: data loading from NVM not finished; “1”: data loading from NVM finished

9.2.3 Status Registers2

This status register is for FIFO, located in address 20H
Register 20H has 4 high bits indicating for FIFO frame counts, 3 low bits indicate for FIFO overrun, FIFO watermark and FIFO full. This status registers is read only.

Table 20. Status Register 2

Addr	7	6	5	4	3	2	1	0
20H	FIFO_FRAME_CNT[3:0]				-	FIFO_OR	FIFO_WM_INT	FIFO_FULL_INT

FIFO_FRAME_CNT[3:0] is used for recording how much data is stored in FIFO memory. And the range of FRAME_CNT is 0~8.

FIFO_OR is triggered when FIFO is full and additional data is written into FIFO. This FIFO_OR can be considered as flag of discarding old data.

FIFO_WM_INT is triggered when the level of buffer reaches the level defined by register FIFO_WTMK (0x2E[5:3]). When FIFO_FRAME_CNT ≥FIFO_WTMK, the flag will be set to 1. And the flag will be set to 0 if FIFO_FRAME_CNT is less than FIFO_WTMK.

FIFO_FULL_INT is triggered when the buffer has been fully filled. In FIFO mode (FIFO_MODE = 1 or 3) or STREAM mode (FIFO_MODE = 2), the fill level is 8; In BYPASS mode (FIFO_MODE = 0) the fill level is 1.

9.2.4 Control Registers1

Control registers 1 is in address 0AH. It sets the operational modes (MODE) and over sampling rate (OSR).

Two bits of MODE registers can transfer mode of operations in the device, the four modes are Suspend Mode, Normal mode, Single Mode, and Continuous Mode. The default mode after Power-On-Reset (POR) is Suspend Mode. Suspend Mode should be added in the middle of mode shifting between Continuous Mode, Single Mode, and Normal Mode.

Over sample Rate (OSR1) registers are used to control bandwidth of an internal digital filter. Larger OSR1 value leads to smaller filter bandwidth, less in-band noise and higher power consumption. It could be used to reach a good balance between noise and power. Four over sample ratio can be selected, 8,4,2 or 1.

Another filter is added for better noise performance; The depth can be adjusted through OSR2. There are totally 5 levels selectable.

Table 21. Control Registers 1

Addr	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0AH	OSR2<2:0>			OSR1<1:0>		-	MODE<1:0>	

Reg.	**Definition**	**00**	**01**	**10**	**11**
Mode	Mode Control	Suspend Mode	Normal Mode	Single Mode	Continuous Mode

Reg.	Definition	00	01	10	11
OSR1	Over Sample Ratio	8	4	2	1

Reg.	Definition	000	001	010	011	100	101	110	111
OSR2	Low Pass Filter	1	2	4	8	16	16	16	16

9.2.5 Control Registers2

Control registers 2 is in address 0BH. It controls soft reset, output data rate and set/reset mode.

Set/Reset Mode can be controlled by the register SET/RESET MODE. There are 3 modes for selection: SET AND RESET ON, SET ONLY ON and SET AND RESET OFF. In SET ONLY ON or SET AND RESET OFF mode, the offset is not renewed during measuring.

Field ranges of the magnetic sensor can be selected through the register RNG. The full-scale range is determined by the application environments. The lowest field range has the highest sensitivity, therefore, higher resolution.

The Output data rate is controlled by ODR registers. Five data update frequencies can be selected: 1Hz, 10Hz, 50Hz, 100Hz or 200Hz.

Soft reset can be done by setting the register SOFT_RST High. Soft reset can be invoked at any time of any mode. After setting High，the SOFT_RST bit will not be auto-cleared. So after the soft reset command 0BH=80, another command 0BH=00 is always needed.

Table 22. Control Registers2

Addr.	7	6	5	4	3	2	1	0
0BH	SOFT_RST	ODR[2:0]			RNG[1:0]		SET/RESET MODE<1:0>	

Reg.	Definition	00	01	10	11
SET/RESET MODE	Set and reset mode control	Set and reset on	Set only on	-	Set and reset off

Reg.	Definition	00	01	10	11
RNG	Full Scale Range(Guass)	32	16	8	32

Reg.	Definition	000	001	010	011	100	101	110	111
ODR	Output data Rate(Hz)	1	10	50	100	200	200	200	200

Reg.	Definition	0	1
SOFT_RST	Soft reset	No reset	Soft reset, restore default value of all registers

9.2.6 Control Registers3

Self-test function is added for verification of the signal-chain. When the function is enable through the bit self-test, an inner-built current is generated and an additional signal is added to the sensor, generating a difference in the 3 axis value.

There are 1 bit reserved for built-in self-test. only when the chip is under Continuous Mode, the self-test bit can be set high to enable the chip to enter self-test Mode; After the self-test is done and self-test is generated, this bit will be auto cleared.

3 bytes are addressed to store the self-test data. They are 13H for X axis,14H for Y axis and 15H for Z axis.

Table 23. Control Registers3

Addr	7	6	5	4	3	2	1	0
0EH	SELFTEST	-	-	-	-	-	-	-

Reg.	Definition	0	1
SELFTEST	Self-test function control	Self-test disable	Self-test enable

9.2.7 Control Registers4

The bit 0x21[4:0] can be set 1 to enable 5 signals used as IBI sources respectively, these 5 signals are data ready, self-test ready, data overflow, FIFO full and FIFO watermark.

Table 24. Control Registers4

Addr	7	6	5	4	3	2	1	0
21H	-	-	-	FF_WM_IEN	FF_FULL_IEN	ST_RDY_IEN	OVFL_IEN	DRDY_IEN

Reg.	Definition	0	1
FF_WM_IEN	FIFO watermark IBI	FIFO watermark IBI disable	FIFO watermark IBI enable

Reg.	Definition	0	1
FF_FULL_IEN	FIFO full IBI	FIFO full IBI disable	FIFO full IBI enable

Reg.	Definition	0	1
ST_RDY_IEN	Selftest data ready IBI	Selftest data ready IBI disable	Selftest data ready IBI enable

Reg.	Definition	0	1
OVFL_IEN	Data overflow IBI	Data overflow IBI disable	Data overflow IBI enable

Reg.	Definition	0	1
DRDY_IEN	Data ready IBI	Data ready IBI disable	Data ready IBI enable

9.2.8 Control Registers5

This register is in address 2EH. It controls FIFO mode, FIFO watermark and FIFO channel selection.

There are three operation modes of FIFO. The FIFO can be configured as FIFO mode, STREAM mode or BYPASS mode.

The FIFO watermark level can be set every 1 step, The upper limit of watermark level is 7. It is prohibited to change FIFO_WTMK [2:0] bits in any other modes than Suspend Mode.

User can enable FIFO function and select data of certain axis to be stored in the FIFO by setting FIFO_CHNL_SEL[2:0]

Table 25. Control Registers5

Addr	7	6	5	4	3	2	1	0
2EH	FIFO_MODE[1:0]		FIFO_WTMK[2:0]			FIFO_CHNL_SEL[2:0]		

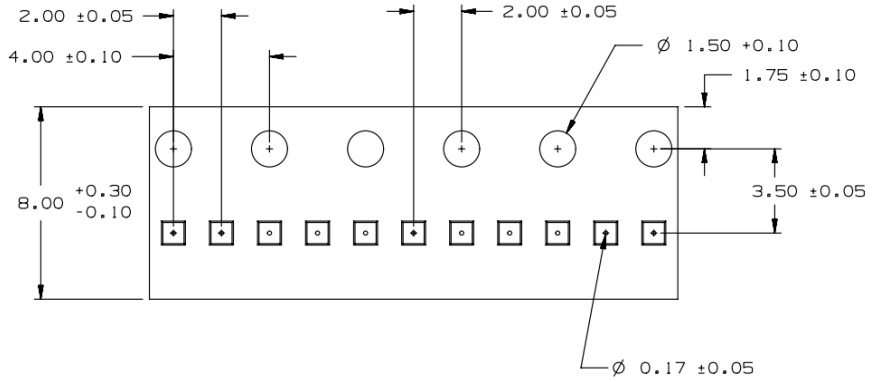
Reg.	Definition	00	01	10	11
FIFO_MODE[1:0]	FIFO MODE	By Pass	FIFO	Stream	FIFO

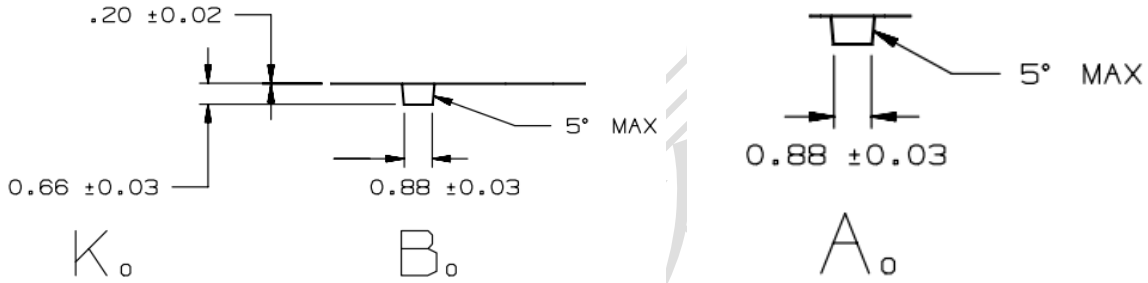
Reg.	Definition	000	001	010	011	100	101	110	111
FIFO_WTMK[2:0]	Watermark level setting	-	1	2	3	4	5	6	7

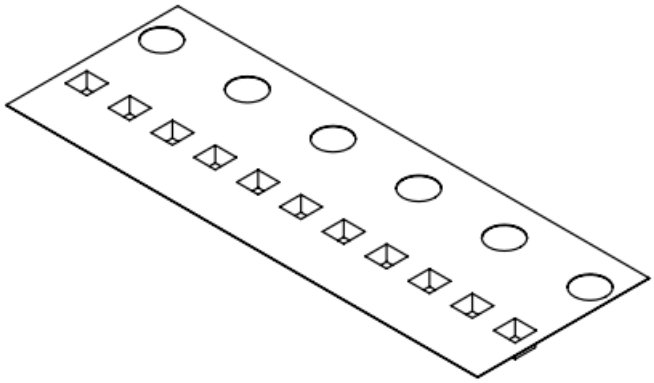
Reg.	Definition	000	001	010	011	100	101	110	111
FIFO_CHNL_SEL [2:0]	FIFO channel setting	FIFO disable	X Only	Y Only	-	Z Only	-	-	XY Z All

10. TAPE AND REEL SPECIFICATION

QMC6309H is shipped in a standard carboard box. The box dimension for 1 reel is: L X W X H = cm x cm x cm. The quantity is 5000pcs per reel, please handle with care

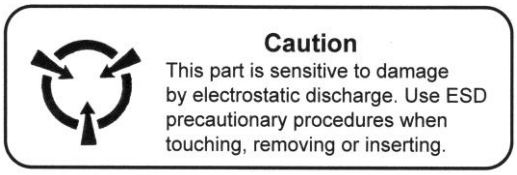






ORDERING INFORMATION

Ordering Number	Operating Temperature	Package	Packaging
QMC6309H	-40°C ~ 85°C	WLCSP	Tape and Reel: 5k pieces/reel



CAUTION: ESDS CAT. 1B

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